

## 75A, 55V, 0.012 Ohm, N-Channel UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75339.

## Ordering Information

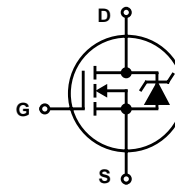
PART NUMBER	PACKAGE	BRAND
HUF75339G3	TO-247	75339G
HUF75339P3	TO-220AB	75339P
HUF75339S3S	TO-263AB	75339S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75339S3ST.

## Features

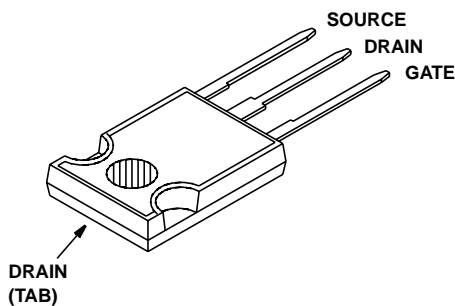
- 75A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER® Models
  - SPICE and SABER Thermal Impedance Models Available on the WEB at: [www.Intersil.com/families/models.htm](http://www.Intersil.com/families/models.htm)
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

## Symbol

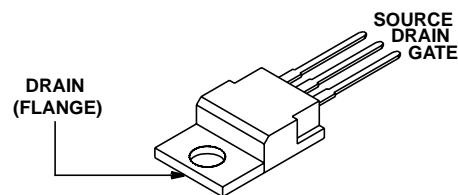


## Packaging

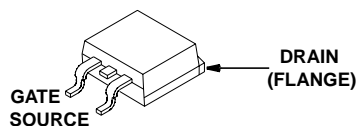
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



# HUF75339G3, HUF75339P3, HUF75339S3S

## Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	55	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	55	V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20$	V
Drain Current			
Continuous (Figure 2) . . . . .	$I_D$	75	A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 4	
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figures 6, 14, 15	
Power Dissipation . . . . .	$P_D$	200	W
Derate Above $25^{\circ}\text{C}$ . . . . .		1.35	$\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $T_J = 25^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ .

## Electrical Specifications $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V (Figure 11)	55	-	-	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V	-	-	1	μA	
		V <sub>DS</sub> = 45V, V <sub>GS</sub> = 0V, T <sub>C</sub> = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r <sub>DS(ON)</sub>	I <sub>D</sub> = 75A, V <sub>GS</sub> = 10V (Figure 9)	-	0.010	0.012	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R <sub>θJC</sub>	(Figure 3)	-	-	0.74	°C/W	
Thermal Resistance Junction to Ambient	R <sub>θJA</sub>	TO-247	-	-	30	°C/W	
		TO-220, TO-263	-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V <sub>GS</sub> = 10V)							
Turn-On Time	t <sub>ON</sub>	V <sub>DD</sub> = 30V, I <sub>D</sub> ≡ 75A, R <sub>L</sub> = 0.4Ω, V <sub>GS</sub> = 10V, R <sub>GS</sub> = 5.1Ω	-	-	110	ns	
Turn-On Delay Time	t <sub>d(ON)</sub>		-	15	-	ns	
Rise Time	t <sub>r</sub>		-	60	-	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>		-	20	-	ns	
Fall Time	t <sub>f</sub>		-	25	-	ns	
Turn-Off Time	t <sub>OFF</sub>		-	-	70	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q <sub>g(TOT)</sub>	V <sub>GS</sub> = 0V to 20V	V <sub>DD</sub> = 30V, I <sub>D</sub> ≡ 75A, R <sub>L</sub> = 0.4Ω I <sub>g(REF)</sub> = 1.0mA (Figure 13)	-	110	130	nC
Gate Charge at 10V	Q <sub>g(10)</sub>	V <sub>GS</sub> = 0V to 10V		-	60	75	nC
Threshold Gate Charge	Q <sub>g(TH)</sub>	V <sub>GS</sub> = 0V to 2V		-	3.7	4.5	nC
Gate to Source Gate Charge	Q <sub>gs</sub>			-	9	-	nC
Reverse Transfer Capacitance	Q <sub>gd</sub>			-	23	-	nC

# HUF75339G3, HUF75339P3, HUF75339S3S

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>CAPACITANCE SPECIFICATIONS</b>						
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 12)	-	2000	-	pF
Output Capacitance	$C_{OSS}$		-	700	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	160	-	pF

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 75\text{A}$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 75\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	85	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 75\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	160	nC

## Typical Performance Curves

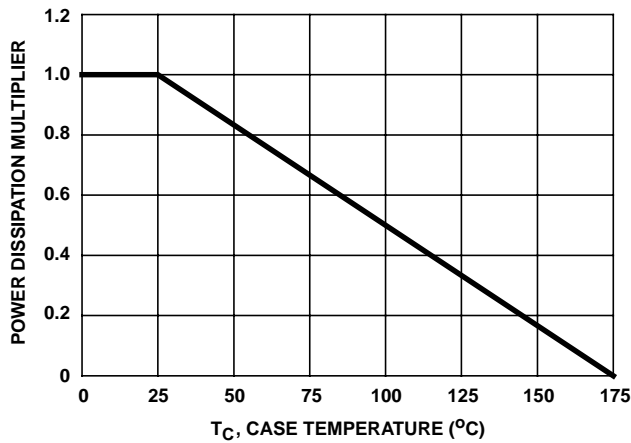


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

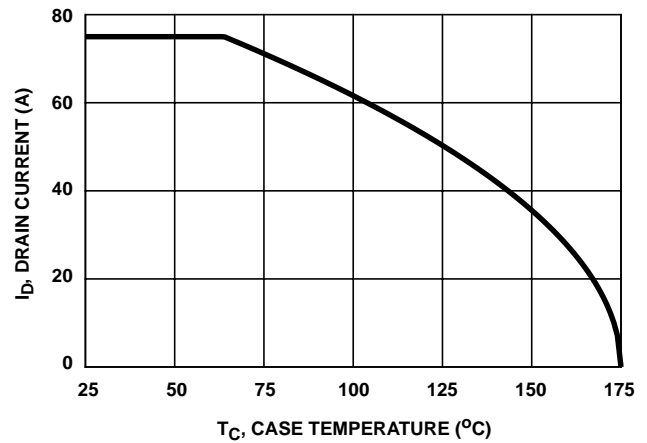


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

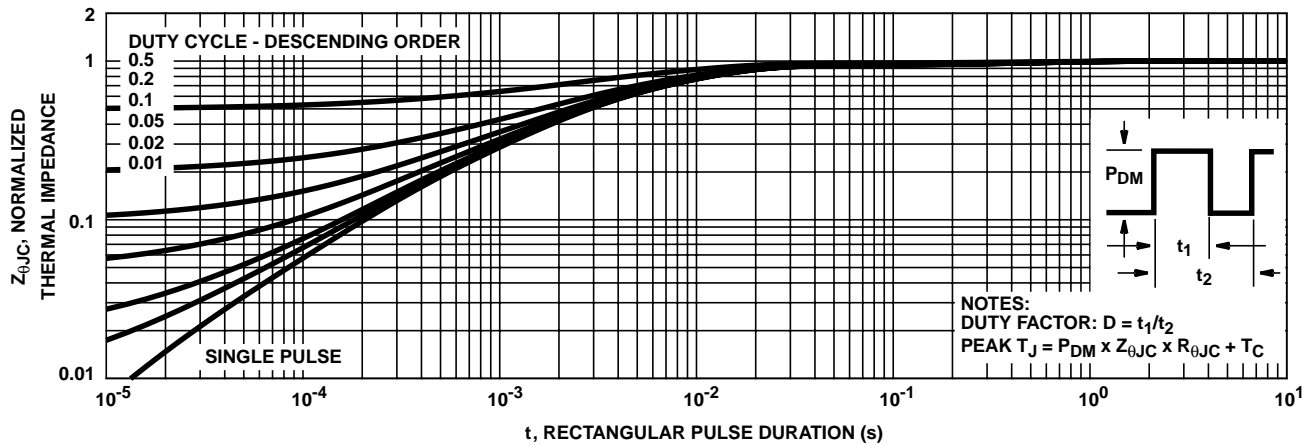


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

# Typical Performance Curves (Continued)

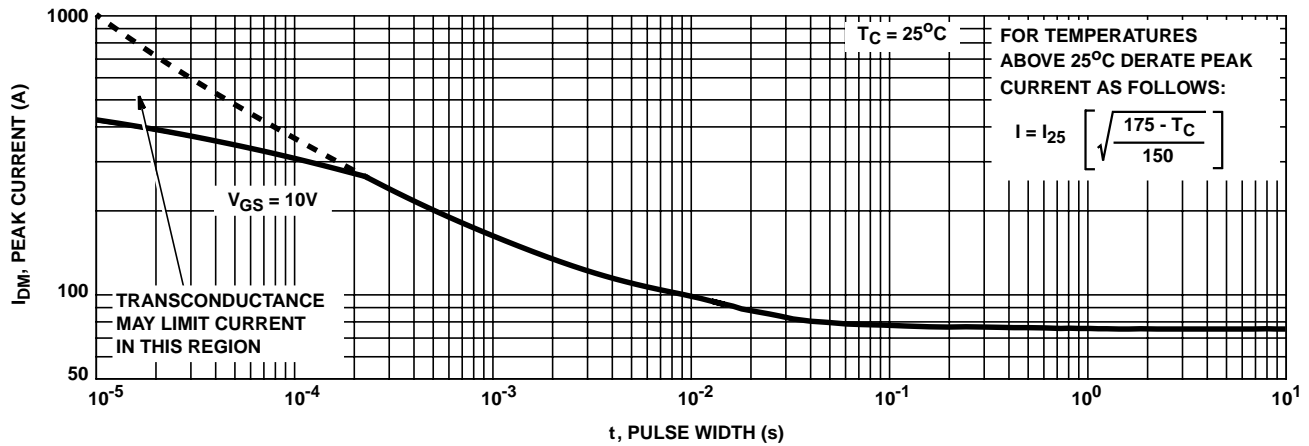


FIGURE 4. PEAK CURRENT CAPABILITY

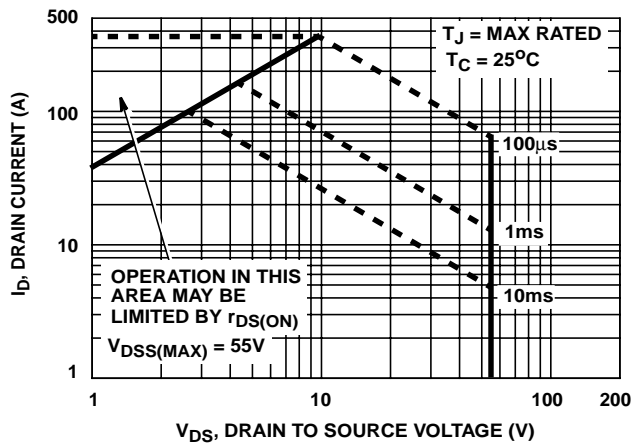
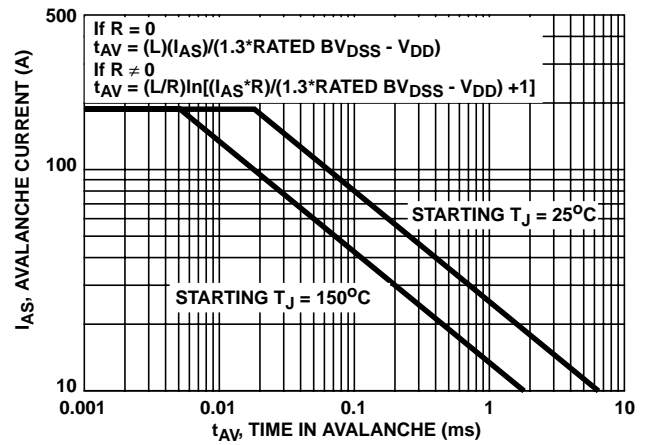


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

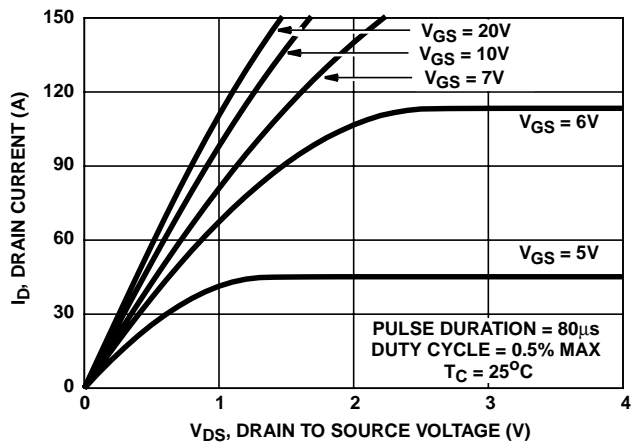


FIGURE 7. SATURATION CHARACTERISTICS

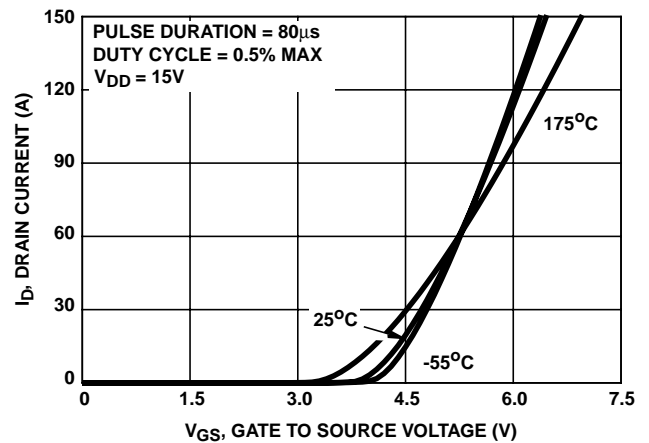


FIGURE 8. TRANSFER CHARACTERISTICS

# Typical Performance Curves (Continued)

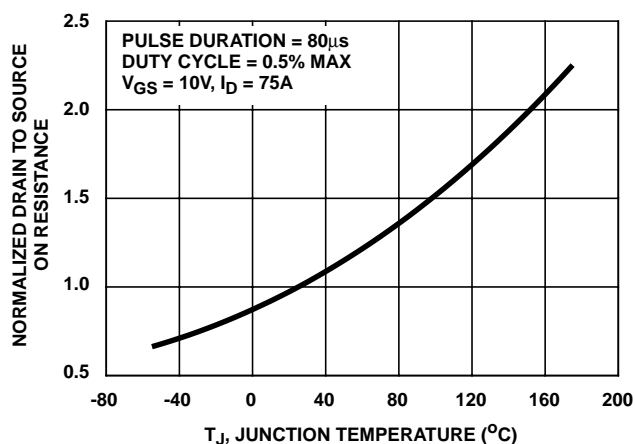


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

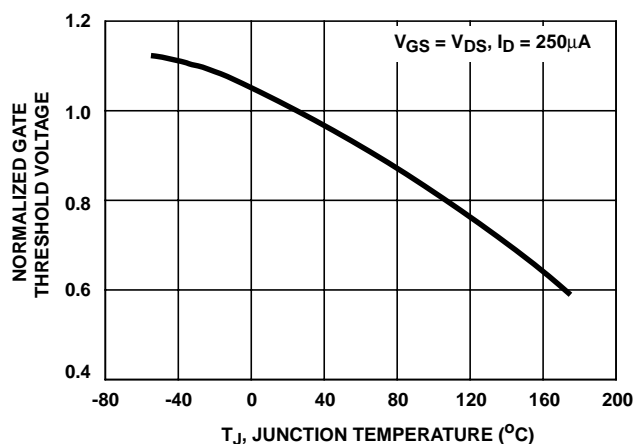


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

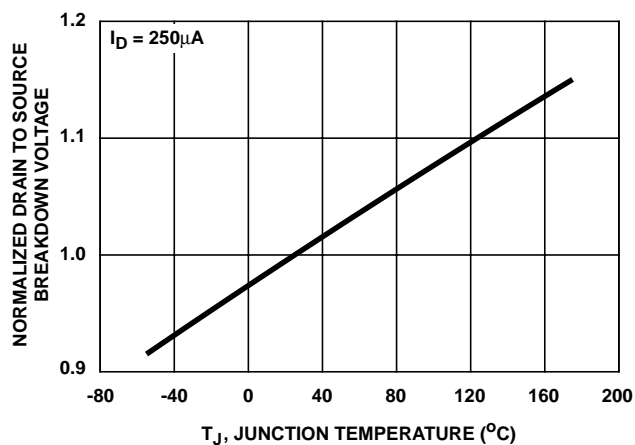


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

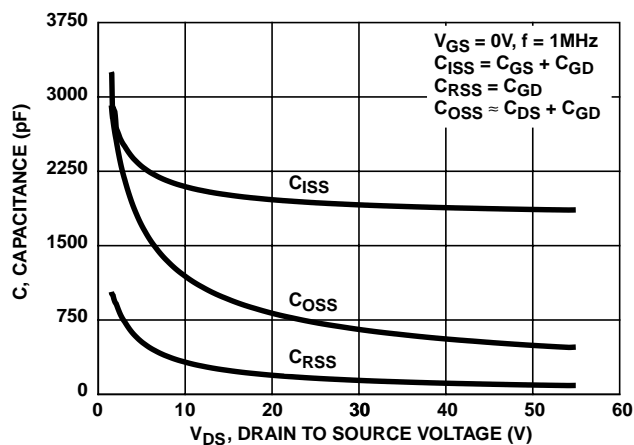
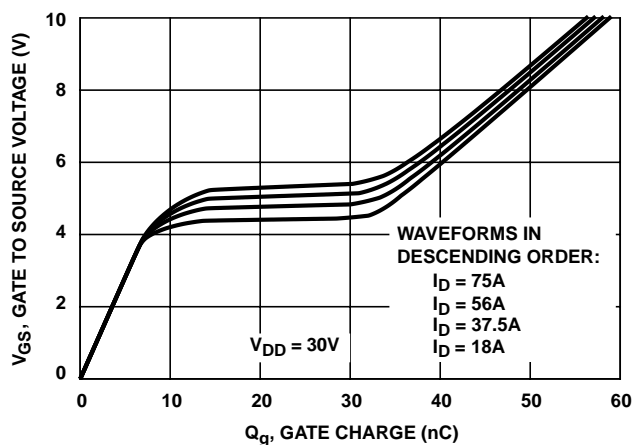


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

# Test Circuits and Waveforms

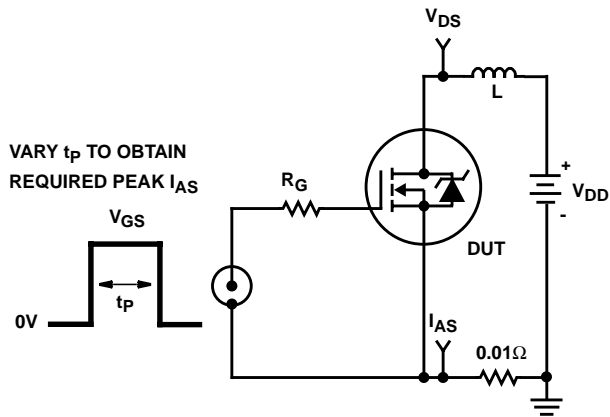


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

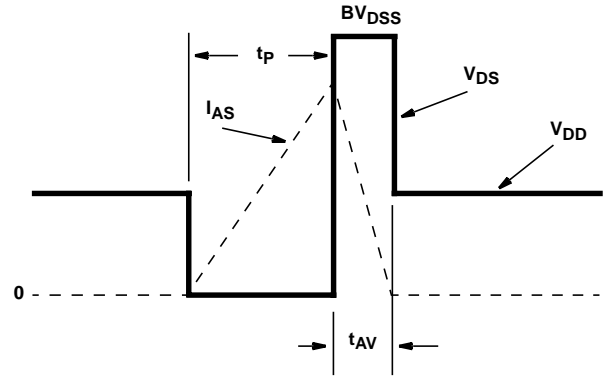


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

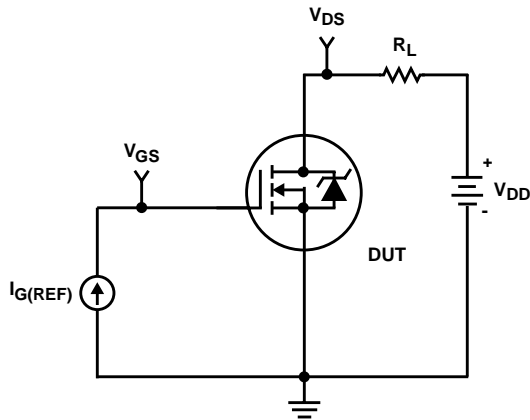


FIGURE 16. GATE CHARGE TEST CIRCUIT

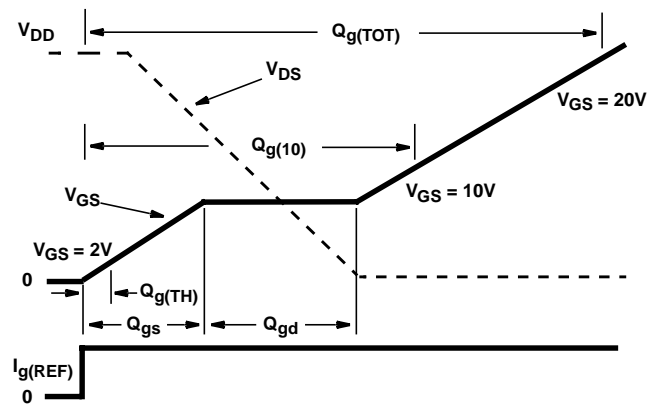


FIGURE 17. GATE CHARGE WAVEFORM

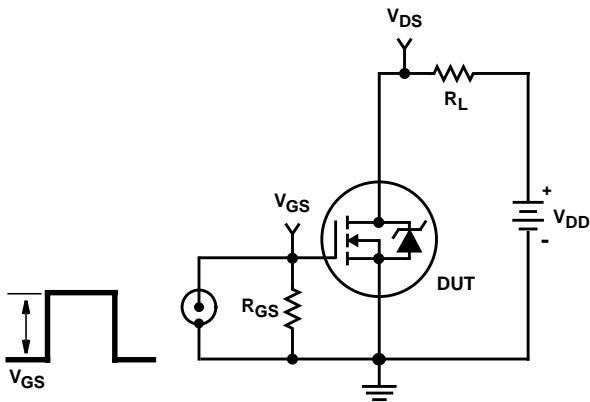


FIGURE 18. SWITCHING TIME TEST CIRCUIT

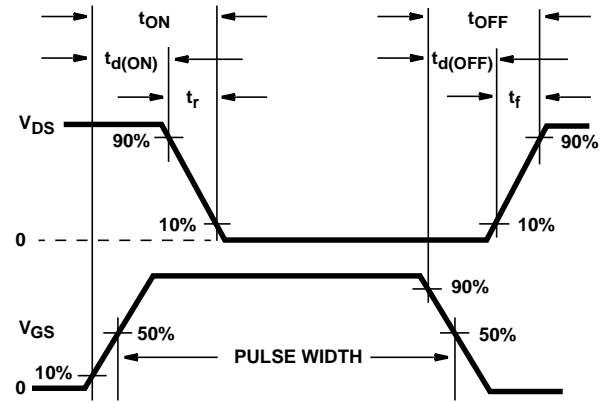


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

## PSpice Electrical Model

.SUBCKT HUF75339 2 1 3 ; rev 23 February 1999

CA 12 8 2.80e-9  
CB 15 14 2.80e-9  
CIN 6 8 1.77e-9

DBODY 7 5 DBODYMOD  
DBREAK 5 11 DBREAKMOD  
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 59.2  
EDS 14 8 5 8 1  
EGS 13 8 6 8 1  
ESG 6 10 6 8 1  
EVTHRES 6 21 19 8 1  
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9  
LGATE 1 9 2.0e-9  
LSOURCE 3 7 4.7e-10  
K1 LSOURCE LGATE 0.0302

MMED 16 6 8 8 MMEDMOD  
MSTRO 16 6 8 8 MSTROMOD  
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
RDRAIN 50 16 RDRAINMOD 1.95e-3  
RGATE 9 20 0.34  
RLDRAIN 2 5 10  
RLGATE 1 9 20  
RLSOURCE 3 7 4.7  
RSLC1 5 51 RSLCMOD 1.0e-6  
RSLC2 5 50 1e3  
RSOURCE 8 7 RSOURCEMOD 6.0e-3  
RVTHRES 22 8 RVTHRESMOD 1  
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
S1B 13 12 13 8 S1BMOD  
S2A 6 15 14 13 S2AMOD  
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

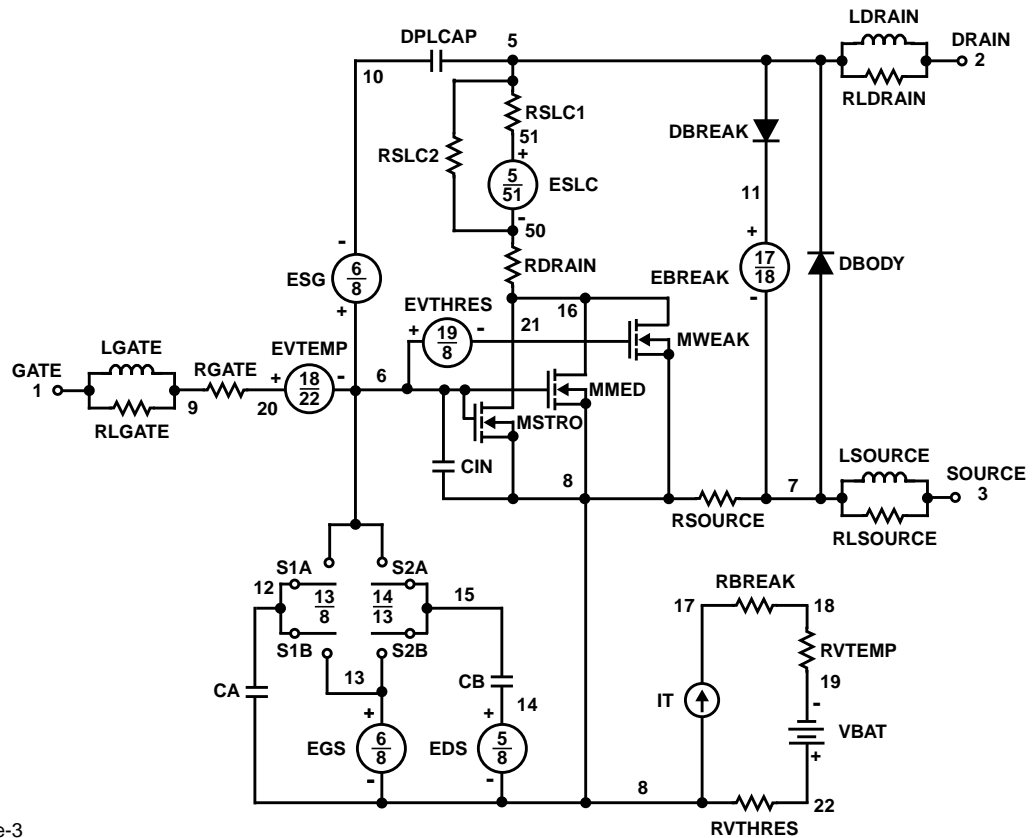
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*230),4))}

.MODEL DBODYMOD D (IS = 3.5e-12 RS = 3.02e-3 N = 1.02 XTI = 5.5 TRS1 = 3.0e-3 TRS2 = 4.0e-6 CJO = 2.9e-9 TT = 4.35e-8 M = 0.5)  
.MODEL DBREAKMOD D (RS = 8.5e-2 TRS1 = 8.0e-4 TRS2 = 1.0e-7)  
.MODEL DPLCAPMOD D (CJO = 2.25e-9 IS = 1e-30 M = 0.8 )  
.MODEL MMEDMOD NMOS (VTO = 3.1 KP = 1.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG=0.34)  
.MODEL MSTROMOD NMOS (VTO = 3.73 KP = 86.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
.MODEL MWEAKMOD NMOS (VTO = 2.7 KP = 0.01 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG=3.4)  
.MODEL RBREAKMOD RES (TC1 = 1.08e-3 TC2 = -2.5e-7)  
.MODEL RDRAINMOD RES (TC1 = 2.05e-2 TC2 = 1.6e-5)  
.MODEL RSLCMOD RES (TC1 = 6.0e-3 TC2 = -2.8e-6)  
.MODEL RSOURCEMOD RES (TC1 = 5.5e-4 TC2 = 1.75e-5)  
.MODEL RVTHRESMOD RES (TC1 = -3.65e-3 TC2 = -6.0e-6)  
.MODEL RVTEMPMOD RES (TC1 = -2.3e-3 TC2 = -4.0e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -9 VOFF= -5.5)  
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.5 VOFF= -9)  
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0 VOFF= 2.1)  
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.1 VOFF= 0)

.ENDS

NOTE: For further discussion of the PSpice model, consult **A New PSpice Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.







## SPICE Thermal Model

REV 11 February 1999

HUF75339

CTHERM1 th 6 5.00e-3  
 CTHERM2 6 5 1.90e-2  
 CTHERM3 5 4 7.95e-3  
 CTHERM4 4 3 9.00e-3  
 CTHERM5 3 2 2.95e-2  
 CTHERM6 2 tl 12.55

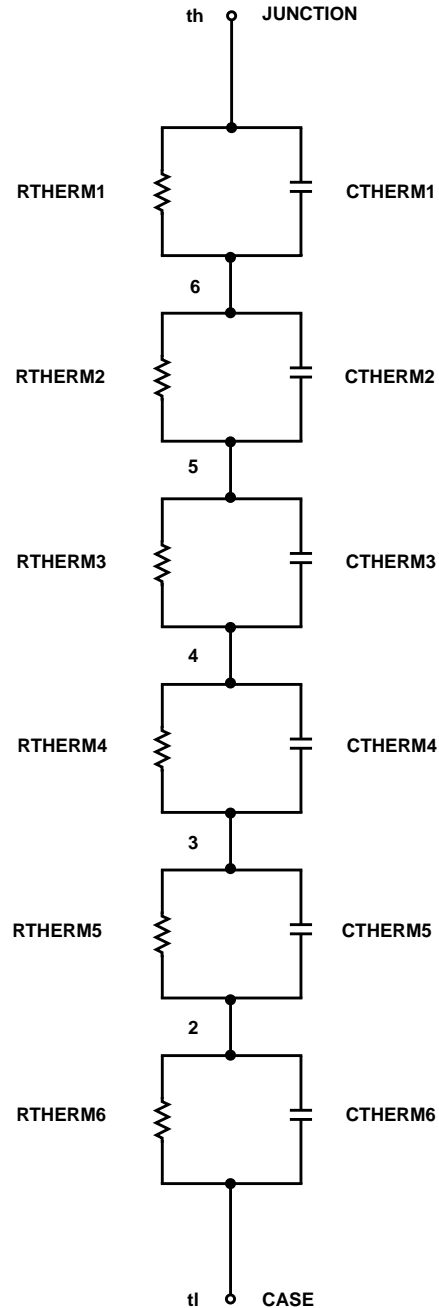
RTHERM1 th 6 5.04e-3  
 RTHERM2 6 5 1.25e-2  
 RTHERM3 5 4 3.54e-2  
 RTHERM4 4 3 1.98e-1  
 RTHERM5 3 2 2.99e-1  
 RTHERM6 2 tl 3.97e-2

## SABER Thermal Model

SABER thermal model HUF75339

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 5.00e-3
    ctherm.ctherm2 6 5 = 1.90e-2
    ctherm.ctherm3 5 4 = 7.95e-3
    ctherm.ctherm4 4 3 = 9.00e-3
    ctherm.ctherm5 3 2 = 2.95e-2
    ctherm.ctherm6 2 tl = 12.55

    rtherm.rtherm1 th 6 = 5.04e-3
    rtherm.rtherm2 6 5 = 1.25e-2
    rtherm.rtherm3 5 4 = 3.54e-2
    rtherm.rtherm4 4 3 = 1.98e-1
    rtherm.rtherm5 3 2 = 2.99e-1
    rtherm.rtherm6 2 tl = 3.97e-2
}
```



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